CLAIMS

What is claimed is:

1. A method of forming a multi-level semiconductor device wiring interconnect structure comprising the steps of:

a) forming a dielectric insulating layer over a conductive portion;

b) forming a via opening in closed communication with the conductive portion;

c) forming a barrier layer to line the via opening;

d) forming a layer of AlCu to fill the via opening to form an AlCu via including a portion overlying the first dielectric insulating layer; and,

e) forming the portion to form an AlCu interconnect line over the AlCu via.

2. The method of claim 1, wherein steps a) through e) are repeated to sequentially form an overlying AlCu via followed by an overlying AlCu interconnect line.

3. The method of claim 1, wherein the AlCu via process is a magnetron sputtering process carried out at a temperature less than about 400 °C.

4. The method of claim 3, wherein the AlCu via process is carried out at pressure less than about 5 milliTorr.

5. The method of claim 1, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

6. The method of claim 1, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

7. The method of claim 1, wherein the barrier layer is selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

8. The method of claim 1, wherein the conductive area comprises silicide electrical contact areas comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions.

9. The method of claim 8, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

10. The method of claim 8, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, or combinations thereof.

11. The method of claim 1, wherein steps a) through f) are repeated to form at least 3 metallization layers over a PMD layer.

12. The method of claim 1, wherein steps a) through f) are repeated to form a multi-level semiconductor device consisting essentially of AlCu wiring.

13. A method of forming a multi-level semiconductor device wiring interconnect structure to improve electrical properties including an electro-migration resistance and electrical resistance comprising the steps of:

a) forming a dielectric insulating layer over a conductive portion;

b) forming a via opening in closed communication with the conductive portion;

c) forming a barrier layer to line the via opening;

d) forming a layer of AlCu at a temperature less than about 400 °C to fill the via opening to form an AlCu via including a portion overlying the first dielectric insulating layer;

e) forming the portion to form an AlCu interconnect line over the AlCu via; and,

f) forming a barrier layer over the AlCu interconnect line.

14. The method of claim 13, wherein steps a) through f) are repeated to sequentially form overlying AlCu vias followed by overlying AlCu interconnect lines through at least 3 metallization level.

15. The method of claim 13, wherein the process is a carried out at pressure less than about 5 milliTorr.

16. The method of claim 13, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

17. The method of claim 13, via openings are formed with an aspect ratio greater than 1.5.

18. The method of claim 13, wherein the barrier layers are selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

19. The method of claim 13, wherein the conductive area comprises salicide electrical contact comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions.

20. The method of claim 19, wherein the salicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

21. The method of claim 19, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.

22. The method of claim 13, wherein steps a) through f) are repeated to form at least 3 metallization layers over a PMD layer.

23. The method of claim 13, wherein steps a) through f) are repeated to form a multi-level semiconductor device consisting essentially of AlCu wiring.

24. A multi-level wiring interconnect structure for a semiconductor device comprising:

a) a dielectric insulating layer over a conductive portion;

b) an AlCu via comprising a first barrier layer formed in the first dielectric insulating layer in closed communication with the conductive portion; and,

c) an AlCu interconnect line comprising a second barrier layer disposed on the AlCu via and over the first dielectric insulating layer.

25. The multi-level wiring interconnect structure of claim 24, wherein structure portions a) through c) are stacked sequentially to comprise at least three metallization layers.

26. The multi-level wiring interconnect structure of claim 24, wherein structure portions a) through c) are stacked sequentially to comprise at least three metallization layers.

27. The multi-level wiring interconnect structure of claim 24, wherein structure portions a) through c) are stacked sequentially to form a multi-level semiconductor device consisting essentially of AlCu wiring.

28. The multi-level wiring interconnect structure of claim 24, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

29. The multi-level wiring interconnect structure of claim 24, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

30. The multi-level wiring interconnect structure of claim 24, via openings are formed with an aspect ratio greater than 1.5.

31. The multi-level wiring interconnect structure of claim 24, wherein the first and second barrier layers are selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

32. The multi-level wiring interconnect structure of claim 24, wherein the conductive portion comprises silicide electrical contact areas comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions.

33. The multi-level wiring interconnect structure of claim 31, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

34. The multi-level wiring interconnect structure of claim 31, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.

35. A multi-level wiring interconnect structure for a semiconductor device comprising:

a) a dielectric insulating layer over a conductive portion;

b) an AlCu via comprising a barrier layer formed in the first dielectric insulating layer in closed communication with the conductive portion;

wherein structure portions a) through b) are stacked sequentially to comprise at least three metallization layers.

36. The multi-level wiring interconnect structure of claim 35, wherein structure portions a) through c) are stacked sequentially to comprise a PMD layer at least three metallization layers.

37. The multi-level wiring interconnect structure of claim 35, wherein structure portions a) through c) are stacked sequentially to form a multi-level semiconductor device consisting essentially of AlCu wiring.

38. The multi-level wiring interconnect structure of claim 35, wherein the dielectric insulating layer is selected from the group consisting of carbon doped silicon oxide, organo silicate glass (OSG), and fluorinated silicate glass (FSG).

39. The multi-level wiring interconnect structure of claim 35, wherein the dielectric insulating layer consists essentially of fluorinated silicate glass (FSG).

40. The multi-level wiring interconnect structure of claim 35, via openings are formed with an aspect ratio grater than 1.5.

41. The multi-level wiring interconnect structure of claim 35, wherein the barrier layers are selected from the group consisting of Ti/TiN, TiN, Ta, TaN, and combinations thereof.

42. The multi-level wiring interconnect structure of claim 35, wherein the conductive portion comprises silicide electrical contact areas comprising a CMOS transistor portion selected from the group consisting of a gate electrode and source and drain regions.

43. The multi-level wiring interconnect structure of claim 42, wherein the silicide electrical contact areas comprise a metal silicide selected from the group consisting of $TiSi_2$ and $CoSi_2$.

44. The multi-level wiring interconnect structure of claim 42, wherein the CMOS transistor forms a portion of a circuit selected from the group consisting of logic circuitry, memory circuitry, analog circuitry, and combinations thereof.